International Journal of Scientific & Engineering Research, Volume 4, Issue 8, August 2013
ISSN 2229-5518

# Design and Analysis of Hybrid Operational Amplifiers Using Poly-Si Thin Film Transistor For Low Voltage Applications

G.Prabhakaran, V.Kannan

**Abstract**— The design of Operational Amplifier in a new technique is presented in this paper, of a Hybrid Thin Film Transistor operational amplifier made by Poly Silicon thin film transistor and MOSFET which operates at 3V power supply. The Operational Amplifier designed is a two-stage Hybrid TFT OPAMP followed by an output buffer. This OPAMP employs a Miller capacitor and is compensated with a current buffer. The unique behaviour of the MOS transistors in saturation region not only allows a designer to work at a low voltage, but also at high frequency. Optimization of one or more parameters may easily result into degradation of others while designing of two-stage op-amps. In this paper we analyze the results of Differential amplifier, Inverting amplifier, Non-Inverting amplifier, Integrator and Differentiator of hybrid operational amplifier, using HSPICE circuit simulator.

**Key Words** —Hybrid, HSPICE, Low Voltage Applications, MOSFET, Operational Amplifier, Poly-Silicon, Thin Film Transistor.

## 1 Introduction

FOR large area electronics, there has been considerable interest to integrate both amorphous silicon (a -Si:H) thin-film transistors (TFTs), for low leakage in the OFF state, and Poly-silicon TFTs, for high drive currents, on the same substrate. This might be done to integrate Poly-silicon drivers in flat panel displays using a-Si: H TFTs in pixels.

A problem with organic TFTs is that they tend to degrade in ambient conditions [4]. High performance interface electronics need operational amplifier as the key building block, which again has proved to be a difficult task, due to extremely low mobility of the TFTs. The op-amp has been built on a-Si:H, since it has a low gain [1, 5].

Op-Amp is among today's most widely used integrated circuit blocks. They can be used to accomplish summers, integrators, differentiators, comparators etc. An Op-amp is a high-gain differential input amplifier and various characteristics of it comprise high CMRR, high PSRR and a high Slew Rate.

This paper is divided into the following sections. In Section 1 we provide a brief introduction of the progress in flexible electronics using Poly-Si, a-Si:H and organic TFTs and the challenges that still remain. In Section 2, we briefly discuss the characteristics of the materials described in this paper. In section 3 we discuss Hybrid TFT op-amp using Poly-Si TFT in combination with MOSFET. In Section 4, we discuss the performance achieved through applications of above said Hybrid Op-Amp and also, the simulation results are presented. Finally we present the conclusion in section 5.

- *Author G.Prabhakaran is Research Scholar in Sathyabama University, Chennai - 600118, Tamilnadu, INDIA. Cell:9841915996 (e-mail: prabhakaran_govind@rediffmail.com).*
- *Co-Author V.Kannan is Principal, Jeppiaar Institute of Technology, Chennai-600118, Tamilnadu, INDIA ( e-mail: drvkannan123@gmail.com)*

## 2 Structure of TFT

Poly silicon thin film transistors (Poly-Si TFT) are becoming more and more important both in microelectronics and in LCD due to its low temperature process. A problem of poly Si TFT is the, presence of an anomalous leakage current (Ion, off current) and this current is depend on the bias and temperature strongly. The anomalous leakage current is the main deficiency of poly Si TFT when used as pixel switches and used in static and dynamic memory. Thus the research on the leakage current characteristics and the reduction leakage current of poly Si TFT is very important.

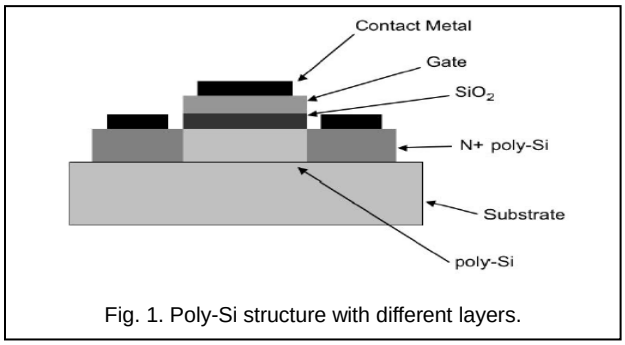


Fig. 1. Poly-Si structure with different layers.

Generally, leakage current is generated from grain boundary defects near the drain. It is regarded; the field-assisted generation mechanism is the main reason of the anomalous leakage current.

Fig.1 shows the structure of Poly Si TFT is a kind of three terminal devices; its substrate is floating just like SOI MOSFET. There exist float body effect. "Kink effect" is a kind of float body effect caused by parasitic bipolar transistor when poly Si TFT works at saturation condition. This kind of parasitic bipolar transistor effect also can exist when poly Si TFT works in the off state and weak inversion region, due to the

field-assisted generation mechanism from trap state in poly Si TFT grain boundary near the region of drain. A simple physics model to describe the parasitic bipolar transistor effect when poly Si TFT works in the off state is developed. By using the model, the relations of leakage current between terminal voltage, temperature of the TFT can be obtained.

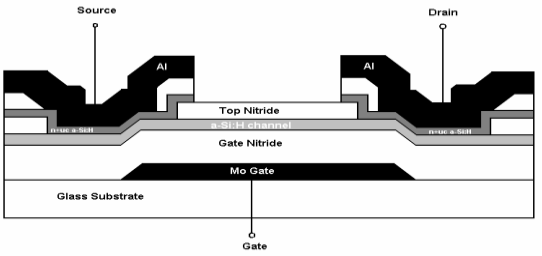


Fig. 2. Cross-section of an a-Si:H TFT.

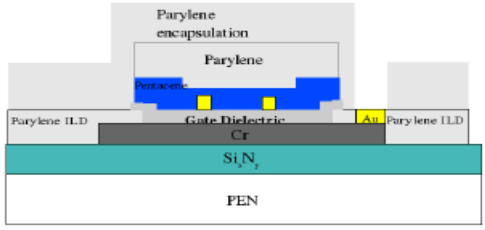


Fig. 3. Pentacene structure with different layers

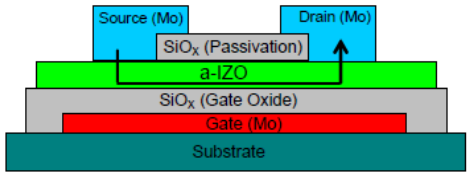


Fig. 2. Structure of ZIO TFTs with the different layers

Fig.2 shows the cross section of a-Si:H TFT, which indicates that it is a three terminal device. It consists of an un-doped a-Si:H layer sandwiched between gate and passivation dielectrics, along with low-resistivity source and drain contacts. Therefore, the TFT has two a- Si:H interfaces. The a-Si:H interface that is deposited before a-Si:H film and closer to the gate terminal is referred to as the front interface. The interface closer to the drain and source terminals are referred to as the back interface. N-channel accumulation mode operation is most commonly used. Equivalent P-channel transistor is not used due to much lower mobility of holes in a-Si, which gives a factor of 100 drain current reduction compared to the N-channel transistor.

Depletion mode devices are prevented by the high defect density of doped material, which makes it difficult to deplete the channel.

The organic p-channel TFTs uses pentacene as the active layer and is deposited at room temperature (see Fig. 3). Aluminum acts as the gate metal and parylene as the gate dielectric [6]. Finally, the devices are encapsulated using a parylene process. The saturation mobility is 0.08 $cm^2/Vs$ with an on/off current ratio greater than $10^4$. Recently, ZnO (and its derivatives) (see Fig. 4) has attracted interest due its higher mobility and electrical stability [2, 3, 18, 19].

## 3 Operational Amplifiers

### 3.1 Related Work

The two-stage CMOS OPAMP is a widely used analog building block in many OPAMP design literatures which is a simple and robust topology providing good values for most of its electrical parameters. The design procedures were proposed for this Op-Amp which reduces the degree of freedom in the design equations, therefore, preventing the possibility to meet optimized performance [7, 8]. Of course, there are electrical parameters which can be improved with circuit arrangements appropriately. A two stage CMOS OPAMP design procedure suitable for pencil-and-paper analysis is given by Palmisano, Palumbo and Pennisi [10]. This procedure is allowed to use the limited range of compensation capacitor (condition for compensation is, CC >> Cgs5). In this design, CC is the compensation capacitor and Cgs5 is a parasitic capacitor of MOSFET in the OPAMP second stage. The design procedure that allows the CC a wider range and it would provide a higher degree of freedom in the trade-off between noise and power consumption have been improved by Mahattanakul and Chutichatuporn [11].

A design procedure for settling time minimisation in multistage OP-AMPs with low power and high accuracy level is proposed by Pugliese, Cappuccino and Cocorullo [12]. When an OPAMP is needed to be operated at a high frequency, there are several limitations which come into the forefront in the existing approaches. The designed OPAMP worked at a low power and low voltage, but it permitted a very low unity gain frequency [13]. Although the simulation [15] done in HSPICE shows an operation at a low power supply and consumes lesser power, but the increase observed in the unity gain frequency which cannot be considered to be noteworthy. The multistage design [16, 17] improves the settling time and gain but leads to the decrease of the phase margin and unity gain frequency. As the supply voltage decreases, it becomes difficult to keep the transistors in saturation with the available voltage [14] and also, settling the time parameter of an OPAMP has to be worked with. The effect of capacitive load on unity gain frequency, noise, speed and power balancing are not considered, in these procedures. In this research work, an OPAMP has been designed which exhibits high unity gain frequency for optimized balancing of phase margin, gain, speed, power, noise and load. Here, the method is proposed to set a higher unity gain frequency of the OPAMP working at a lower supply voltage. This permits the value of each circuit element of the amplifier (i.e transistor aspect ratios, bias current and compensation capacitor) to be related to the required electrical parameters.

### 3.2 Operational Amplifiers on TFTs

The op-amp design, described in this paper, is that of a classic two stage CMOS op-amp. Fig. 5 gives the schematics, with n-channel inputs. We show that the design give moderate gain and a relatively low unity gain frequency (UGF). Based on the design in Fig. 5, an optimized Hybrid op-amp with Class A driver are at its output. The theoretical gain and UGF of this amplifier is given as where and denote the trans-conductance of the p-channel and n-channel devices respectively, and denotes the output conductance of the devices respectively. To achieve stability in closed-loop conditions and clear of closed-loop wavering, two-stage CMOS operational amplifiers adopt Miller compensation which is necessary in OPAMP design [7, 9].

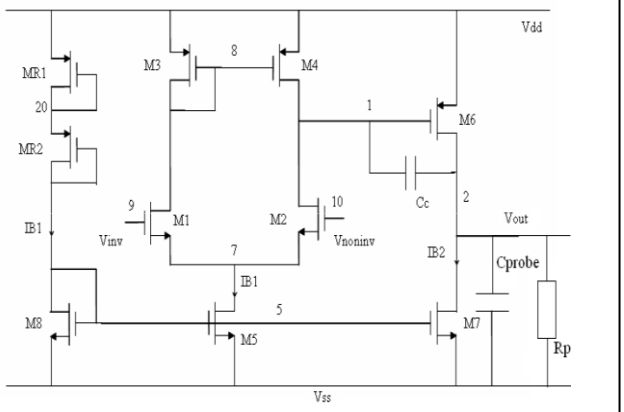


Fig. 5. Two Stage CMOS Op-amp with n-channel input

The Chip with p-channel input stage followed by n-channel 2nd stage. The op-amp has a pMOS differential input stage followed by an n-channel cascoded common source stage. The 2nd stage is cascoded to provide the necessary gain. The reason for choosing a p-channel input stage is with greater bandwidth and slew rate.

The precision and flexibility of the operational amplifier is a direct result of the use of negative feedback. Op-amplifiers employing feedback will have superior operating characteristics at a sacrifice of gain. With enough feedback, the closed loop amplifier characteristics become a function of the feedback elements. In the typical feedback circuit, the feedback elements are two resistors. The precision of the "closed loop" gain is set by the ratio of the two resistors and is practically independent of the "open loop" amplifier. Thus, amplification to almost any degree of precision can be achieved with ease. CMOS is known for lower power consumption. But this advantage is true only for slower amplifiers.

### 3.3 Hybrid Op-Amp using Poly-Si TFT

Like the characteristics of CMOS devices, TFTs are having high noise immunity and low static power consumption. Significant power is drawn only when the transistors in the MOS and TFT devices are switching between on and off states. Also, this device won't produce much heat as other forms of logic. These devices also allow a high density of logic functions on a chip.

Compare to other FETs, the TFT have higher pinch-off voltage. The TFT acts as a switch in most applications: the transistor is typically switched on for tens of microseconds and then switched off for tens of milliseconds.

In our previous paper [20], we have analyzed and modeled the hybrid op-amp using a-Si TFT with p-channel MOSFET is shown in Fig.6. a-Si TFT is used as n-type FET (M1, M2, M5, M7 and M8) and p-channel MOSFET (M3, M4, M6, M9 and M10) is used as p-type TFT.

In this paper, using the Fig.6, we have used the Poly-Si TFT as n-type FET (M1, M2, M5, M7 and M8) and p-channel MOSFET (M3, M4, M6, M9 and M10) is used as p-type TFT. Fig.12 shows its input and output waveforms in common mode configuration.

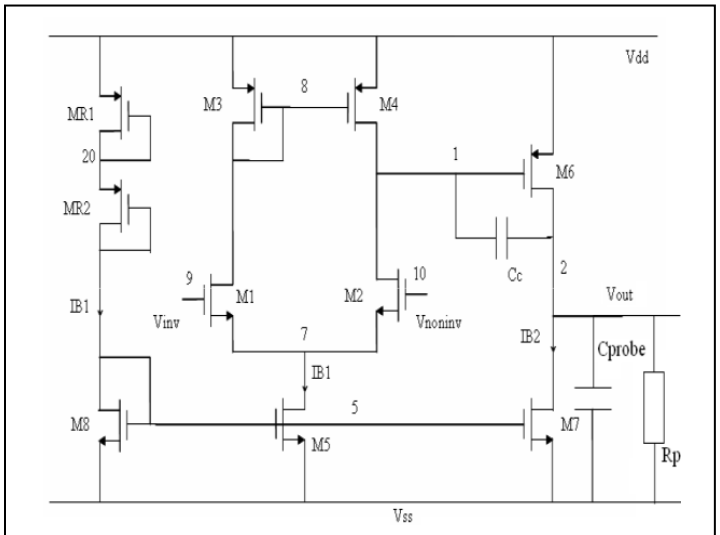


Fig. 6. Two stage Hybrid op-amp with n-channel input

### 3.4 The Various Stages Incorporated in the Design of Op-Amp

Presently optimizing all parameters in a design has become necessary. In the past few years, we have come across various new-fangled topologies and have been employed in various applications. In this design, we have chosen a simple differential pair amplifier for input amplifier, common source amplifier for output amplifier, and a current mirror circuit as a biasing circuit.

The topology of the circuit designed is that of a standard CMOS op-amp in Fig.6. It comprised of three stages of circuits, namely differential gain stage, additive gain stage and bias strings. Examining these stages further will provide valuable insight into the operation of this amplifier.

*Differential Gain Stage of Op-Amp*

The first stage of interest is the differential gain stage which consists of transistors M1 to M4. Transistors M1 and M2 are Poly Si TFT (as NMOS) transistors which form the basic input stage of the amplifier. The gates of M1 and M2 are the inverting input and the non-inverting input respectively. According to the gain of the differential stage, a differential input signal applied across the two input terminals will be amplified. The

trans-conductance of this stage is equivalent to the trans-conductance of M1 or M2. The PMOS transistorsM3 and M4 are the active load transistors of the differential amplifier. The three distinguishable advantages of current mirror active load used in this circuit are: 1. the use of active load devices creates a large output resistance in a relatively small amount of die area, 2. the current mirror topology performs the differential to single-ended conversion of the input signal, and 3. the load also helps with common mode rejection ratio.

***Additive Gain Stage of Op-Amp***

The purpose of this additive gain stage, is to provide additional gain in the amplifier. This stage consisting of transistors M6 (Poly Si TFT) and M7 (PMOS), takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. This stage employs an active device M6, similar to the differential gain stage, to serve as the load resistance for M5 (Poly Si TFT). The trans-conductance of this stage is simply the trans-conductance of M7.

***Bias String of Op-Amp***

Biasing of this operational amplifier is achieved with only four transistors. Transistor M8 (Poly Si TFT) and the current source (diode of M9 and M10) supply a voltage between the gate and source of M7, diode of M9 and M5. Transistors M7 and M5 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. Diode of M8 is connected to ensure it operates in the saturation region. Biasing of the other transistors in the circuit (M1 – M4 and M6) is properly controlled by the node voltages present in the circuit itself. Most importantly, M6 is biased by the gate to source voltage (VGS) set up by the VGS of the current mirror load.

## 4 CIRCUIT CONFIGURATION

In this paper, we are discussing about the following configuration of Hybrid Op-Amp using Poly Si TFT:

1. Inverting Amplifier
2. Non- Inverting Amplifier.
3. Differential Amplifier
4. Differentiator
5. Integrator.

### 4.1 Inverting Amplifier

Fig.7 shows the design of Inverting amplifier. The positive end of the input voltage $V_{in}$ is connected through a resistor $R_1$ to the inverting input pin (-) on the op-amp (the negative end of $V_{in}$ is connected to ground) shown in Fig.7. The non-inverting input pin (+) is connected to ground. The gain $A_f$ of the amplifier is defined as the ratio of the output to input voltages.

$$A_f = \frac{V_{out}}{V_{in}}$$

When $V_{out}$ and $V_{in}$ in the above equation represent the actual values of the output and input voltages. When the input is a sinusoidal AC signal, the output will be a sinusoidal AC signal.

For the above circuit, we can assume that the same current flows through both resistors because of the extremely high input impedance and that the voltage at the inverting pin is nearly the same as ground. Thus

$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

so that the gain will be

$$A_f = -\frac{R_f}{R_1}$$

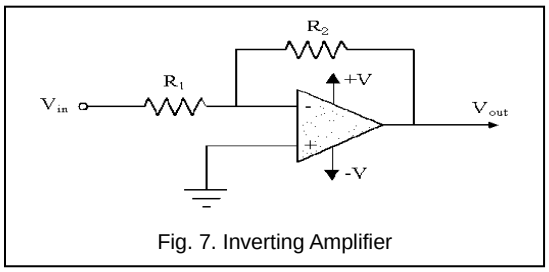


Fig. 7. Inverting Amplifier

In the above equation, when the input and output are sinusoidal AC signals, the negative sign indicates a 180-degree phase shift between the output and input.

***Inverting Amplifier Using Hybrid Op- Amp***

As we have applied input to the inverting terminal of hybrid op-amp so it is known as inverting amplifier and Fig.13 shows its input and output waveforms.

### 4.2 Non Inverting Amplifier

Fig.8 shows a simple design for a non-inverting amplifier. The input voltage $V_{in}$ is applied directly to the non-inverting terminal of the op-amp. The two external resistors $R_1$ and $R_2$ are providing Negative feedback which form a voltage divider and apply a fixed fraction of the output voltage to the inverting input terminal of the op-amp. The gain is determined by the external resistors $R_1$ and $R_2$ according to the equation:

$$A_f = 1 + \frac{R_2}{R_1}$$

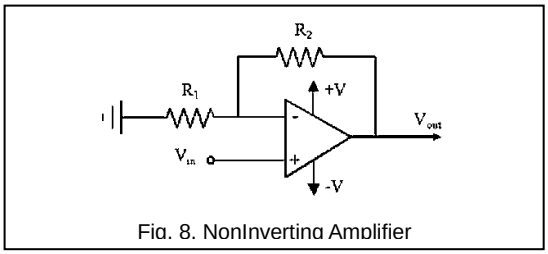


Fig. 8. NonInverting Amplifier

***Non- Inverting Amplifier Using Hybrid Op-Amp***

As we have applied input to the non-inverting terminal of hybrid op-amp so it is known as non-inverting amplifier. Fig.14 shows its input and output waveforms.

### 4.3 Differential Amplifier

There is only one input signal in the previous two circuits (inverting and non-inverting amplifiers). A differential amplifier is used to deal with two input signals and only the difference between the two input signals is amplified. The circuit shown in Fig.9 is a simple differential amplifier.

Notice the two resistors connected to $V_1$ and $V_2$ should have the same value (well-matched resistors), and another two resistors, one connected between $V_{out}$ and inverting terminal and another one connected to ground and non-inverting terminal of Op-amp, should also have the same value. According to the following equation, the output signal is related to the two input signals:

$$V_{out} = \frac{R_2}{R_1} V_{in}$$

The gain of the differential amplifier is the ratio between $V_{out}$ and $(V_2 - V)_1$:

$$A_f = \frac{V_{out}}{V_2 - V_1} = \frac{R_2}{R_1}$$

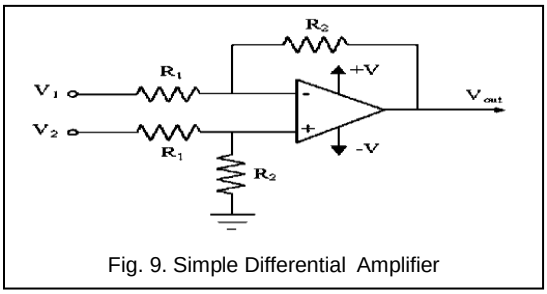


Fig. 9. Simple Differential Amplifier

***Differential Amplifier Using Hybrid Op-Amp***

As we have applied input to both the non-inverting and inverting terminal of hybrid op-amp, so it is known as differential amplifier. Fig.15 shows its input and output waveforms.

### 4.5 Differentiator

A differentiator circuit produces an output that is proportional to the derivative or rate of change of the input voltage over time. Differentiator circuit can be constructed with a resistor, and a capacitor as shown in the Fig.10. The output signal is related to the input signals according to the following equation:

$$V_{out} = -RC \frac{dV_{in}}{dt}$$

Since the output voltage of a differentiator is proportional to the input frequency, high frequency signals may saturate or cut-off the amplifier. For this reason: a resistor can be placed in series with the capacitor in the input. This establishes high frequency limit beyond which differentiation no longer occurs:

$$f_B = \frac{1}{2\pi R_{in} C_{in}}$$

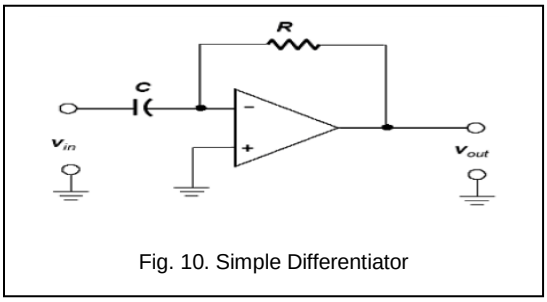


Fig. 10. Simple Differentiator

A feedback capacitor is added in parallel with the feedback resistor to achieve greater attenuation at higher frequencies or prevent oscillation. This establishes another break frequency that can be calculated.

***Differentiator Using Hybrid Op-Amp***

As we have applied input to the inverting terminal of op-amp using TFT, so it is known as inverting amplifier. Fig.16 shows its input and output waveforms.

### 4.6 Integrator

An integrator circuit in which the output voltage waveform is the integral of the input voltage waveform. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor $R_f$ is replaced by a capacitor $C_f$. The expression for the output voltage is given as,

$$V_{out} = -\left(\frac{1}{R_f C_f}\right) \int V_i dt$$

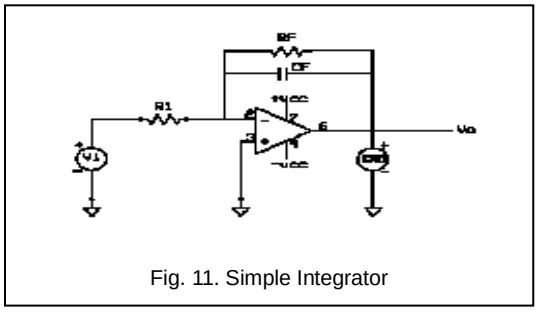


Fig. 11. Simple Integrator

Here the negative sign indicates that the output voltage is 180° out of phase with the input signal. Normally between $f_a$ and $f_b$ the circuit acts as an integrator. Generally, the value of $f_a < f_b$.

The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is, $T \geq R_f C_f$. An Integrator circuit can be constructed with an operational amplifier, a resistor, and a capacitor as shown in the Fig.11.

***Integrator Using Hybrid Op-Amp***

As we have applied input to the inverting terminal of op-amp using TFT, so it is known as inverting amplifier. Fig.17 shows its input and output waveforms.

## 5 Results And Discussion

The proposed model is verified by simulation program with Integrated Circuit Emphasis (HSPICE) is used to simulate and compare with the results predicted by the analytical model.

Fig.12 shows the input and output waveforms of Hybrid Op-amp using Poly-Si TFT in common mode configuration. Fig.13 shows the input and output waveforms of Inverting Amplifier. Fig.14 shows the input and output waveforms of Non-inverting Amplifier. Fig.15 shows the input and output waveforms of Differential Amplifier. Fig.16 shows the input and output waveforms of Differentiator. Fig.17 shows the input and output waveforms of Integrator.

W and L values calculated for various MOSFET/TFTs used in this circuit as shown in Table 2.

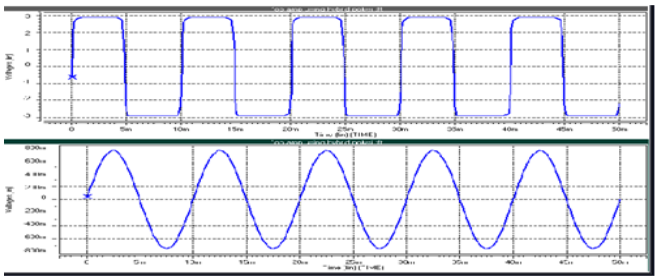

Fig. 12. (a) Input applied in non-inverting input and their corresponding output

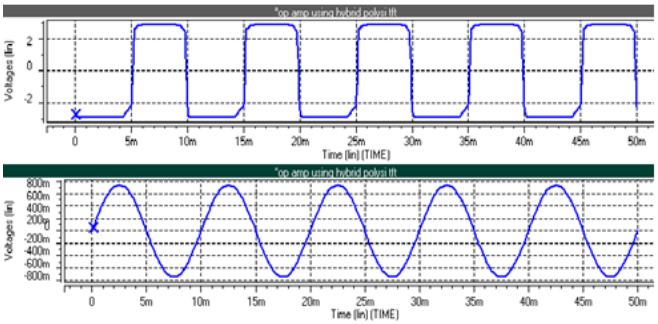


Fig. 12. (b) Input applied in inverting input and their corresponding

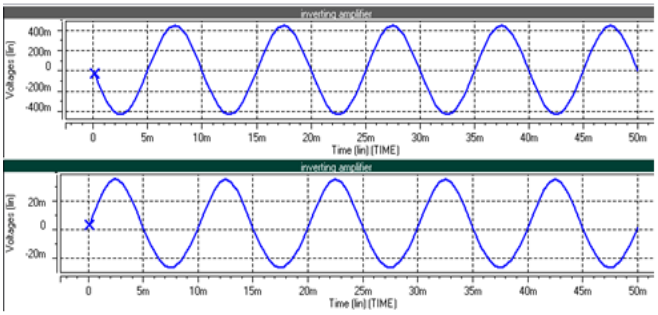


Fig. 13. Simulation results of Inverting Amplifier using Hybrid Op-Amp

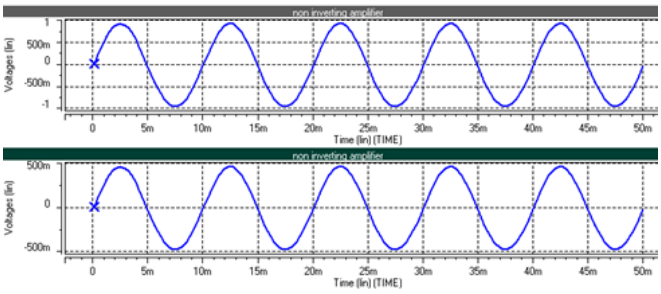


Fig. 14. Simulation results of Non- Inverting Amplifier using Hybrid Op-Amp

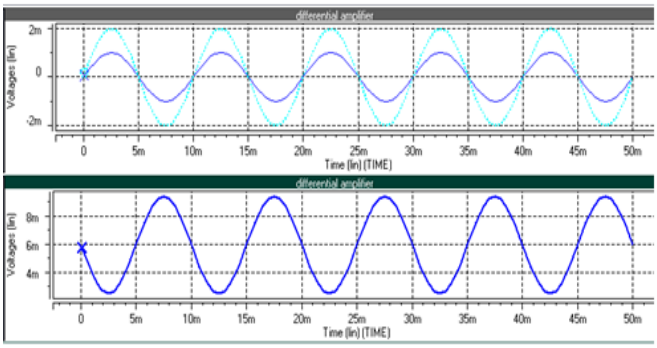


Fig. 15. Simulation results of Differential Amplifier using Hybrid Op-Amp

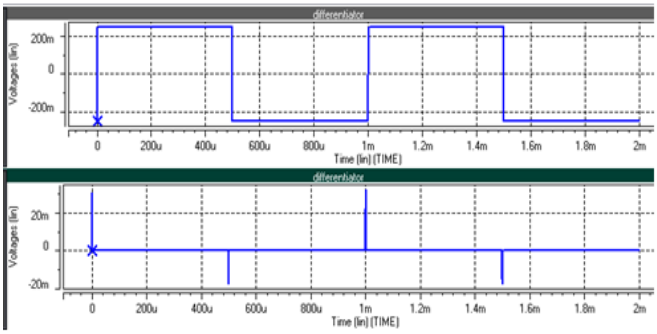


Fig. 16. Simulation results of Differentiator using Hybrid Op-Amp

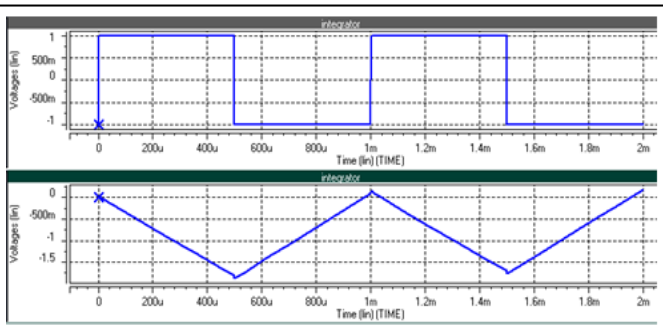


Fig. 17. Simulation results of Integrator using Hybrid Op-Amp

Following are the required specifications, has been used for simulation:

TABLE 1
SPECIFICATIONS, USED FOR SIMULATION

| PARAMETER | SPECIFICATION |
|---|---|
| VDD | 3V |
| VSS | -3V |
| VIN | 1.5V SIN (0 0.75 100) |
| CC | 0.6P |
| RL | 5K |

TABLE 2
W AND L VALUES OF MOSFET / TFTS

| MOSFET/ TFT | W (µm) | L (µm) | MOSFET/ TFT | W (µm) | L (µm) |
|---|---|---|---|---|---|
| M1 | 10 | 1 | M6 | 80 | 1 |
| M2 | 10 | 1 | M7 | 90 | 1 |
| M3 | 8 | 1 | M8 | 40 | 1 |
| M4 | 8 | 1 | M9 | 8 | 1 |
| M5 | 40 | 1 | M10 | 8 | 1 |

The agreement between the model (Fig.6) and simulated results proves the accuracy of the model.

## 6 CONCLUSION

In this paper we have simulated the hybrid Op-Amp using Poly-Si TFT. We have also discussed the basic configurations of Hybrid operational amplifier using Poly-Si TFT and MOSFET. We provide a brief introduction of the progress in flexible electronics using a-Si:H, Poly-Si and organic TFTs. We have discussed the performance achieved through applications of above said Hybrid Op-Amp such as inverting amplifier, non-inverting amplifier, differential amplifier, differentiator and integrator. The simulation results are presented. The simulation results show excellent agreement with existing practical work.

## REFERENCES

[1] Allee, D.R., Clark, L.T., Vogt, B., Shringarpure, R., Venugopal, S.M., Uppili, S.G., Kafthanoglu, K., Shivanlingaiah, H., Li, Z., Fernando, J.J.R., Bawolek, E., O"Rourke, S.M., 2009 "Circuit Level Impact of a-Si:H Thin-Film Transistor Degradation effects," *IEEE Trans. Electron Devices*, 56, pp. 1166-1176.

[2] Venugopal, S.M. and Allee, D.R., 2007, " Integrated a-Si:H source drivers for 4 QVGA electrophoretic display on flexible stainless steel substrate", *IEEE Journal of Display Technology*, 3, pp. 57-63.

[3] Shringarpure, R., Clark, L.T., Venugopal, S.M., Allee, D.R., and Uppili, S.G., 2008, "Amorphous Silicon Logic Circuits on Flexible Substrates", *Proceedings of 2008 IEEE Custom Integrated Circuits Conference*, Sept. 21-24, 2008, San Jose, California.

[4] Sebastian, S., Meerheim, R., Walszar K. and Leo, K., 2008, "Chemical degradation mechanisms of organic semiconductors". *Proc. SPIE- Organic Optoelectronics and Photonics III*, P L. Heremans Ed., 6999, pp: 1-B1-1B10.

[5] Tarn, Y.C., Ku, P.C., Hsieh, H.H. and Lu, L.H., 2010, "An Amorphous Silicon Operational Amplifier and its Application to 4 Bit Digital to Analog Converter," *IEEE J. Solid State Circuits*, 45, pp. 1028-1035.

[6] Allee, D.R., Venugopal, S.M., Krishna, R., Kafthanoglu, K., Quevedo, M., Gowrishankar, S., Avendano-Bolivar, A.E., Alshareef, H.N., Gnade, B., 2009, "Flexible CMOS and Electrophoretic Display," *Society for Information Displays, International Symposium Digest of Technical papers*, June 2009, San Antonio, Texas, pp: 45-54.

[7] D.A Johns and K. Martin, "Analog Integrated Circuit Design", New York *John Willey*, 1997.

[8] Gregorian R., and Temes, G.C. "Analog MOS Integrated Circuits for Signal Processing", John *Wiley and Sons*, 1986.

[9] G. Palmisano and G. Palumbo "A compensation strategy for two-stage CMOS OPAMPs based on current buffer", *IEEE trans. Circuits sys.I, Fundam. Therory Appl.*, vol.44, no. 3, pp 257-262, Mar 1997

[10] G. Palmisano, G. Palumbo and S. Pennisi "Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial", *Analog Integrated Circuits and Signal Processing*, 27, 179–189, 2001.

[11] Mahattanakul, J. and Chutichatuporn, J. (2005) " Design Procedure for Two-Stage CMOS OPAMP with Flexible Noise-Power Balancing Scheme". *IEEE Transaction on Circuits and Systems-I Regular Paper* 52, pp. 1508-1514.

[12] Pugliese, A , Cappuccino, G. and Cocorullo, G. (2008) " Design Procedure for Settling Time Minimization in Three-Stage Nested Miller Amplifiers". *IEEE Transaction on Circuits and Systems-II* 55, pp. 1-5.

[13] R. Kr. Baruah, "Design of a low power low voltage CMOS Opamp", *International Journal of VLSI design & communication systems*, vol. 1, no. 1, mar-2010.

[14] R.Gonzalez, B.M. Gordon, M.A Horowitz, "Supply and Threshold voltage scaling for low power CMOS", *IEEE journal of solid state Electronics*, Vol sc 32, No 8, June 1997.

[15] Ehsan Kargaran, Hojat Khosrowjerdi and Karim Ghaffarzadegan, "A 1.5 V High Swing Ultra- Low-Power Two Stage CMOS OP-AMP in 0.18 µm Technology. 2010 *2nd International Conference on Mechanical and Electronics Engineering (ICMEE 2010).*

[16] Mohammad Taherzadeh-Sani and Anas A. Hamoui,"A 1-V Process-Insensitive Current Scalable Two-Stage Opamp With Enhanced DC Gain and Settling Behavior in 65-nm Digital CMOS", *IEEE Journal of Solid State Circuits*, Vol. 46, No. 3, Mar-2011.

[17] Anshu Gupta and D.K. Mishra, R. Khatri," A Two Stage and Three Stage CMOS OPAMP with Fast Settling, High DC Gain and Low Power Designed in 180nm Technology", *Digital Object Identifier*: 10.1109/CISIM.2010.5643497 (CISIM 2010), pp. 448 – 453, Nov.2010.

[18] Hoffman, R., Emery, T., Yeh, B., Koch, T. and Jackson, W., 2009: "Zinc Indium Oxide Thin-Film Transistors for Active-Matrix Display Backplane", in *SID Symp. Int. Tech. Papers*, May 2009, pp. 288-291.

[19] Wang, Y.Lin, Lim, F.R.W., Norton, D.P., Pearton, S. J., Kravchenko, I.I. and Zavada, J.M., 2007: "Room Temperature Deposited Indium Zinc Oxide Thin Film Transistors," *Appl Phys. Lett.*, 90, pp. 232103.1-232103.3.

[20] G.Prabhakaran, and Dr.V.Kannan: "Analysis And Modelling of Hybrid Operational Amplifiers Using Amorphous Silicon Thin Film Transistor", *CiiT International Journal of Programmable Devices Circuits and Systems*, Vol 3, No 12, September 2011, Print: ISSN 0974 – 973X & Online: ISSN 0974 – 9624.